REMARKS

Claims 1, 3, 8-11 and 12-13 are pending. Claim 1 has been amended to clarify that the external connecting terminal provided on a back surface of the supporting substrate is electrically connected to the conductive pattern "through the substrate." No new matter has been added. Claim 12 is a new dependent claims reciting a semiconductor wherein "said terminal is electrically connected to the conductive pattern through the substrate by a via hole." New claim 13 recites a similar feature. Support for such new claims can be found, for example, in FIG. 1A and page 6, lines 17 to 18 of the application. No new matter has been added.

Specification

The office action has indicated that the title of the invention is not descriptive.

Applicants have amended the title to read: "A Hollow Airtight Semiconductor Device Package ~~and Manufacturing Method thereof~~."

Applicants respectfully assert that the new title is more indicative of the invention to which the claims are directed.

Claim Rejections 35 USC 103

Claims 8-11 were rejected under 35 USC 103(a) as being unpatentable over Prior art figures 9A-9B, Ozimek et al., Sasano and in further view of Toshiba.

The office action cites the Hyoudo patent and suggests that it teaches an "external connecting terminal provided on a back surface of the supporting substrate and electrically connected to the conductive pattern through the substrate" as recited in claim 8. (See page 4, lines 11-15 of the non-final office action)

However, applicants respectfully submit that the Hyoudo patent is not valid prior art for the following reasons.

First, the applicants respectfully point out that the Hyoudo patent is not valid prior art because the current application has an effective filing date earlier than a publication date of the Hyoudo patent. In particular, the Hyoudo patent was filed on April 25, 2000 and claims priority

to a Japanese application filed on April 27, 1999. Although not indicated on the face of the Hyoudo patent, it has a publication date of November 7, 2000 which is 18 months from the priority date of April 27, 1999. (See attached Abstract of the Hyoudo patent labeled Exhibit VII) The present application was filed on September 26, 2001, and claims priority to a Japanese application filed on October 10, 2000. Thus, the present application has an effective filing date of October 10, 2000 which is earlier than the Hyoudo patent publication date of November 7, 2000. Accordingly, the Hyoudo patent is not valid prior art under 35 USC 102(a).

Second, applicants respectfully point out that the Hyoudo patent is not prior art to the present invention because the alleged prior art and the present invention were subject to an obligation of assignment at the time of their inventions were made and they have been assigned to the same entity.

35 USC §103(c) states:

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Furthermore, MPEP 706.02(k) states: "Effective November 29, 1999, subject matter which was prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e) is now disqualified as prior art against the claimed invention if that subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person."

The Hyoudo patent qualifies as possible prior art under 102(e)(1)/103 because it was filed April 25, 2000 and issued on April 2, 2002. The present invention was filed on September 26, 2001. However, because both inventions were subject to an obligation of assignment to Sanyo Electric Company, Ltd. at the time the inventions were made, the Hyoudo patent is not prior art to the present invention. As evidence for the existence of the common assignee, Sanyo Electric Corporation, Ltd., copies of Notice of Recordation of the Assignments for the Hyoudo patent and for the present invention are enclosed respectively as Exhibits I and II. Moreover, all of the inventors of Hyoudo patent and all of the inventors of the present invention are employees of Sanyo Electric Company, Ltd. and all were subject to an obligation of assignment at the time of

the inventions were made. This is evidenced by Exhibits III and IV, which are copies of the original assignments as filed for the Hyoudo patent and the present invention, respectively. Therefore, the Hyoudo patent is not prior art to the present invention. To further support applicants position, applicants have attached Exhibit V (verified statement of the foreign priority document of the present invention) and Exhibit VI (verified translation of the foreign priority document of the present invention).

Claims 1 and 3 were rejected under 35 USC 103(a) as being unpatentable over Prior art figures 9A-9B in view of Ozimek et al. (5,382,310), Toshiba KK[Toke] (JP 07225391A) and Sasano (US 6,313,525 B1).

Claim 1 has been amended to recite an external connecting terminal provided on a back surface of the supporting substrate and electrically connected to the conductive pattern "through the substrate." This feature is based on claim 8 and does not present new issue or new matter. As explained above regarding claim 8, the office action suggests that the Hyoudo patent may teach this feature. However, the Hyoudo patent is not valid prior art for the reasons above, and thus claim 1 should be allowable because none of remaining prior art references teach or suggest feature. Thus, claim 1 should be allowable for at least this reason.

In addition, the prior art references fail to teach or suggest the claimed invention for the following reasons.

With respect to claim 1, the office action asserts that it would have been obvious to one of ordinary skill in the art to modify the device structure of alleged Prior Art Figures 9A-9B, by incorporating the adhesive of Ozimek, the light shielding adhesive resin of Toshsiba and the glass plate, adhesive and external connection of Sasano to maintain air tightness.

Applicants respectfully assert that the teachings of Toshiba are incompatible with Sasano and Ozimek. In particular, although Sasano patent may mention that air tightness is important, it is still directed to an imaging device that includes a **transparent** sealing plate 9 bonded to the upper surface of the package body 1 through **transparent** adhesive 10 (column 5, lines 57 to 61). Ozimek et al. shows an image sensor 10 that includes **transparent** adhesive 26 bonded to a glass plate 28 (column 3, lines 9-31).

In contrast, Toshiba discloses an electrically conductive adhesive film 36 composed of a **non-transparent** adhesive resin and electrically conductive particles for making electrical connections. The devices of Sasano and Ozimek are directed to imaging devices and require **transparent** layers to allow light to enter the devices to operate properly. Therefore, one skilled in the art would not have been led or motivated to combine the teachings of Sasano and Ozimek having a **transparent** adhesive with the teachings of Toshiba having a **non-transparent** adhesive. Accordingly, claims 1 and 3 are non-obvious over the prior-art.

Moreover, the LCD structure of the Toshiba invention is so dissimilar with Sasano's hollow package structure or Figs. 9A and 9B's structure that a person of ordinary skill in the art would not have been led or motivated to combine the disclosure of Toshiba with either Sasano or the admitted prior art. Even if the references are combined, there is no suggestion or teaching in any of the prior art references to use the light shielding adhesive resin as claimed in claim 1. Claims 1, 3 and 12 are thus non-obvious for the foregoing reasons.

Claim 8 includes features similar to claim 1. For the reasons explained above for claim 1, claim 8 should be allowable. Since claims 9-11 and 13 depend from claim 8, claims 9-11 and 13 should be allowable for at least the same reasons as claim 8.

EXHIBIT I

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SEPTEMBER 25, 2000

PTAS

101427781A

WENDEROTH, LIND & PONACK, L.L.P.
CHARLES R. WATTS, ESQ.
2033 K STREET, N.W., SUITE 800
WASHINGTON, DC 20006

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NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

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RECORDATION DATE: 07/20/2000

REEL/FRAME: 010976/0187
NUMBER OF PAGES: 3

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
HYOUDO, HARUO

DOC DATE: 05/15/2000

ASSIGNOR:
KIMURA, SHIGEO

DOC DATE: 05/15/2000

ASSIGNEE:
SANYO ELECTRIC CO., LTD.
5-5, KEIHAN-HONDORI 2-CHOME
MORIGUCHI CITY, OSAKA, JAPAN

SERIAL NUMBER: 09557964
PATENT NUMBER:

FILING DATE: 04/25/2000
ISSUE DATE:

MARY BENTON, EXAMINER
ASSIGNMENT DIVISION
OFFICE OF PUBLIC RECORDS

FORM PTO-1595 (modified)

08-10-2000

101427781

SHEET

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

To the Honorable Assistant Secretary and Commissioner of Patents and Trademarks: Please record the attached original document(s) or copy(ies) thereof.

1. Name of conveying party(ies):

Haruo HYOUDO and Shigeo KIMURA

Additional name(s) of conveying party(ies) attached? NO

2. Name and address of receiving party(ies):

Name: SANYO ELECTRIC CO., LTD.

Street Address: 5-5, Keihan-Hondori 2-chome, Moriguchi City, Osaka, Japan

Additional name(s) & address(es) attached? NO

3. Nature of conveyance: 7-20-00

X Assignment
__ Security Agreement
__ Other ____
__ Merger
__ Change of Name

Execution Date: May 15, 2000

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: ____

A. Patent Application No.(s)
09/557,964

B. Patent No.(s)

Additional numbers attached? NO

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: WENDEROTH, LIND & PONACK, L.L.P.
Attn: Charles R. Watts , Esq.

Street Address: 2033 K Street, N.W., Suite 800

City: Washington, State: DC ZIP: 20006

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 3.41). $40.00

X Enclosed (Check No. 39028)
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9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Charles R. Watts , Reg. No. 33,142
Name of Person Signing

Signature

July 20, 2000
Date

Total number of pages including cover sheet: 3

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EXHIBIT II

CTM

UNITED STATES PATENT AND TRADEMARK OFFICE

Under Secretary of Commerce For Intellectual Property and Director of the United States Patent and Trademark Office
Washington, DC 20231
www.uspto.gov

DECEMBER 05, 2001

PTAS

FISH & RICHARDSON P.C.
CHRIS T. MIZUMOTO
45 ROCKEFELLER PLAZA, SUITE 2800
NEW YORK, NY 10111

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RECORDATION DATE: 09/26/2001

REEL/FRAME: 012209/0616
NUMBER OF PAGES: 4

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
HYODO, HARUO

DOC DATE: 09/17/2001

ASSIGNOR:
KIMURA, SHIGEO

DOC DATE: 09/17/2001

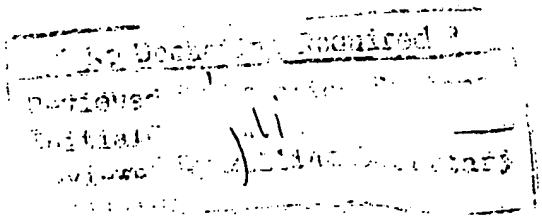
ASSIGNOR:
TAKANO, YASUHIRO

DOC DATE: 09/17/2001

ASSIGNEE:
SANYO ELECTRIC CO., LTD.
5-5, KEIHANHONDORI 2-CHOME
MORIGUCHI-SHI, OSAKA 570-8677,
JAPAN

SERIAL NUMBER: 09963267
PATENT NUMBER:

FILING DATE: 09/26/2001
ISSUE DATE:



MARCUS KIRK, EXAMINER
ASSIGNMENT DIVISION
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10-04-2001

101864556

Substitute Form PTO-1595
Attorney Docket No.: 10417-101001
Client's Ref. No.: F51-136645M/TOM

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Haruo Hyodo, Shigeo Kimura and Yasuhiro Takano

09/26/01

Additional name(s) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):

Sanyo Electric Co., Ltd.
5-5, Keihanhondori 2-chome,
Moriguchi-shi, Osaka 570-8677
Japan

J1040 U.S. PTO
09/963267
09/26/01

Additional names/addresses attached? ☐ Yes ☒ No

3. Nature of conveyance:

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☐ Merger
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☐ Change of Name
☐ Other:

Execution Date: 09/17/2001

4. Application number(s) or patent number(s):

09/963267

If this document is being filed with a new application, the execution date of the application is: 09/17/2001

A. Patent Application No(s).:

B: Patent No(s).:

Additional numbers attached? ☐ Yes ☒ No

5. Name/address of party to whom correspondence concerning document should be mailed:

CHRIS T. MIZUMOTO
Fish & Richardson P.C.
45 Rockefeller Plaza, Suite 2800
New York, New York10111

6. Total number of applications/patents involved: 1

7. Total fee (37 CFR §3.41): $40

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☐ Authorized to charge Deposit Account.

8. Deposit Account No.: 06-1050

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Chris T. Mizumoto
Reg. No. 42,899
Name of Person Signing

Signature

September 26, 2001
Date

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September 26, 2001
Date of Deposit

Valentin Figueroa
Signature

Valentin Figueroa
Typed Name of Person Signing Certificate

FISH & RICHARDSON P.C.
フィッシュ・アンド・リチャードソン法律事務所

Assignment
譲渡

ここにその受領と充足性が確認された善良で価値ある配慮の故に、文末に署名した者は、

For good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the undersigned hereby assign(s) over to:

SANYO ELECTRIC CO., LTD.

(住所)

Having the address:

5-5, Keihanhondori 2-chome,
Moriguchi-shi, Osaka, Japan

(以下「譲渡人」と呼ぶ)と、その承継人および譲受人に対して、

(hereinafter designated as the "ASSIGNEE"), its succesors and assigns, the entire right, title, and interest for the United States in the invention, and all applications for patent and any Letters Patent which may be granted thereof, including said application, and all United States Letters Patents which may be granted thereof, and all divisions, reissues, continuations, and extensions thereof, the said interest being the entire ownership of said Letters Patent when granted to be held by said ASSIGNEE, its succesors, assigns, or their legal repreesentatives, to the full end of the term for which said Letters Patent may be granted, as fully and entirely as the same would have been enjoyed by assignor(s) if this assignment had not been made, the application being known by the title:

(発明の名称)

SEMICONDUCTOR DEVICE AND
MANUFACTURING METHOD THEREOF

弁護士要録番号:

Attorney Docket no.:

という名称で知られ、以下に署名した者が以下に記した日にアメリカ合衆国特許を申請した発明のアメリカ合衆国におけるすべての権利、権原および利権、ならびにその発明に対して行われるすべての特許申請とそれらによって得られる特許状ならびにそれらの分割、再申請、継続および延長を譲渡するものであり、さらにその利権は、当該特許状が譲受人、継承人、さらにその譲受人らまたは彼らの法的代理人に与えられたときに、当該特許状の全所有権をこの譲渡が行われなかった場合に譲渡人に当該特許状が与えられることにより譲渡人が受けたであろう期間の最後の日まで、完全無欠に授けられるものとする。この書状が、申請と同時に登録されない場合は、以下の認識情報が執行後に追加されるものとする。

for the which the undersigned has/have executed an application for patent in the United States of America on the same day herewith. Where this instrument is not filed concurrently with the application, the following identifying information may be added after execution:

シリアル・ナンバー　　登録年月日:

Serial No.　　Filing Date:

Assignment
譲渡

1. 文末に署名した者は、上記の申請、またはその継続出願、一部継続出願、さしかえ出願、分割出願、更新出願、再審査出願、または再発行出願、またはあらゆる修正、抵触審査手続の延長、又はその他権原を譲受人が確保するために必要なあらゆる文書を署名、執行することに同意する。

1. The undersigned hereby agree(s) to sign and execute any further documents and instruments which may be necessary, lawful and proper in the prosecution of said above-nmaed application or in the preparation and prosecution of any continuing, continuation-in-part, substitute, divisional, renewal, reexamination or reissue application or in any amendments, extension of interference proceedings, or otherwiese secure the title thereto to the ASSIGNEE.

2. 文末に署名した者は、工業所有権の保護に関する国際条約または同様な条約のクレームまたは条項に関連して必要となるすべての文書を署名、執行し、必要な行為を行うことに同意する。

2. The undersigned hereby agree(s) to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property of similar agreements.

3. 文末に署名した者は、譲受人に有効な米国特許を取得させるために必要なすべての積極的な行為を実行することに同意する。

3. The undersigned hereby agree(s) to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the ASSIGNEE.

4. 文末に署名した者は、アメリカ合衆国の特許庁長官に対して、当該特許申請またはそれに基づくすべての分割、継続申請から生じるすべての特許状を当該譲受人に発行するように、請願する。

4. The undersigned hereby authorize(s) and request(s) teh Commisioner of Patents in the United States to issue any and all Letters Patents resulting from the said application or any division or divisions or continuing application thereof to the ASSIGNEE.

5. 文末に署名した者は、本状の登記に当りアメリカ合衆国特許庁の規則に従って必要であり、望ましいような識別情報をこの譲渡書に挿入する権利をフィッシュ・アンド・リチャードソン法律事務所に委任するものとする。

5. The undersigned hereby grant(s) to the firm of Fish & Richardson P.C. the power to insert on this agreement any further identification which may be necessary or desirable in order to comply with the rules of the United States patent and Trademark Office for recordation of this document.

Assignment
譲渡

以上を確認のうえで、下記の者が下記の氏名に並んで記された日に各自、署名して本書を発効させるものである。

IN WITNESS THEREBY, executed by the undersigned on the date(s) opposite the undersigned Name(s)

年月日	氏名(楷書):	Date	Typed Name
		September 17, 2001	Haruo Hyodo Haruo HYODO
		September 17, 2001	Shigeo KIMURA Shigeo KIMURA
		September 17, 2001	Yasuhiro TAKANO Yasuhiro TAKANO

以上を確認のうえで、下記の者が下記の氏名に並んで記された日に各自、署名して本書を発効させるものである。

This assignment may be signed before a U.S. notary Public or before at least two witnesses who also sign here:

年月日	氏名(楷書):	Date	Typed Name

EXHIBIT III

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) and other good and valuable consideration paid to each of the undersigned

Insert Name(s) of Inventor(s)

Haruo HYOUDO

Shigeo KIMURA

the undersigned hereby sell(s) and assign(s) to

Insert Name(s) of Assignee(s)

SANYO ELECTRIC CO., LTD.

Address

of 5-5, Keihan-Hondori 2-Chome, Moriguchi City, Osaka, Japan

(hereinafter designated as the Assignee) the entire right, title and interest for the United States as defined in 35 USC 100, in the invention known as

Title of Invention

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

for which an application for patent in the United States has been executed by the undersigned on

Date of Signing Application

May 15, 2000

The undersigned agree(s) to execute all papers necessary in connection with this application and any continuing, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

The undersigned agree(s) to execute all papers necessary in connection with any interference which may be declared concerning this application or continuation, division or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such interference.

The undersigned agree(s) to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

The undersigned agree(s) to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

The undersigned hereby authorize(s) and request(s) the Commissioner of Patents to issue any and all Letters Patents of the United States resulting from said application or any division or divisions or continuing or reissue applications thereof to the said Assignee, as Assignee of the entire interest, and hereby covenants that he has (they have) full right to convey the entire interest herein assigned, and that he has (they have) not executed, and will not execute, any agreement in conflict herewith.

The undersigned hereby grant(s) the firm of WENDEROTH, LIND & PONACK, L.L.P., 2033 K Street, N.W., Suite 800, Washington, DC 20006, the power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent Office for recordation of this document.

In witness whereof, executed by the undersigned on the date(s) opposite the undersigned name(s).

Date May 15, 2000, Name of Inventor 兵藤治雄 Haruo HYOUDO

Date May 15, 2000, Name of Inventor 木村茂夫 Shigeo KIMURA

Date _____, Name of Inventor _____

Date _____, Name of Inventor _____

Date _____, Name of Inventor _____

Date _____, Name of Inventor _____

(This assignment should preferably be acknowledged before a United States Consul. If not, then the execution by the Inventor(s) should be witnessed by at least two witnesses who sign here.)

Witness 境 彦

Witness 渋谷隆生

ACKNOWLEDGMENT

_____
_____ } SS

This _____ day of _____, 19_____, before me

personally came the above-named _____

_____

_____

to me personally known as the individual(s) who executed the foregoing assignment, who did acknowledge to me that he (they) executed the same of his (their) own free will for the purposes therein set forth.

_____
Official Signature

SEAL

_____
Official Title

The above application may be more particularly identified as follows:

U.S. Application Serial No. _____ Filing Date _____

Applicant Reference No._____ Atty. Docket No._____

Title of Invention _____

_____

EXHIBIT IV

Substitute Form PTO-1595
Attorney Docket No.: 10417-101001
Client's Ref. No.: F51-136645M/TOM

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Haruo Hyodo, Shigeo Kimura and Yasuhiro Takano

Additional name(s) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):

Sanyo Electric Co., Ltd.
5-5, Keihanhondori 2-chome,
Moriguchi-shi, Osaka 570-8677
Japan

Additional names/addresses attached? ☐ Yes ☒ No

3. Nature of conveyance:

☒ Assignment
☐ Merger
☐ Security Agreement
☐ Change of Name
☐ Other:

Execution Date: 09/17/2001

4. Application number(s) or patent number(s):

If this document is being filed with a new application, the execution date of the application is: 09/17/2001

A. Patent Application No(s).:

B: Patent No(s).:

Additional numbers attached? ☐ Yes ☒ No

5. Name/address of party to whom correspondence concerning document should be mailed:

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6. Total number of applications/patents involved: 1

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For good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the undersigned hereby assign(s) over to:

SANYO ELECTRIC CO., LTD.

(住所)

Having the address:

5-5, Keihanhondori 2-chome,
Moriguchi-shi, Osaka, Japan

(以下「譲渡人」と呼ぶ)と、その承継人および譲受人に対して、

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(発明の名称)

SEMICONDUCTOR DEVICE AND
MANUFACTURING METHOD THEREOF

弁護士要録番号:

Attorney Docket no.:

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for the which the undersigned has/have executed an application for patent in the United States of America on the same day herewith. Where this instrument is not filed concurrently with the application, the following identifying information may be added after execution:

シリアル・ナンバー　　登録年月日:

Serial No.　　Filing Date:

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1. The undersigned hereby agree(s) to sign and execute any further documents and instruments which may be necessary, lawful and proper in the prosecution of said above-nmaed application or in the preparation and prosecution of any continuing, continuation-in-part, substitute, divisional, renewal, reexamination or reissue application or in any amendments, extension of interference proceedings, or otherwiese secure the title thereto to the ASSIGNEE.

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3. 文末に署名した者は、譲受人に有効な米国特許を取得させるために必要なすべての積極的な行為を実行することに同意する。

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5. The undersigned hereby grant(s) to the firm of Fish & Richardson P.C. the power to insert on this agreement any further identification which may be necessary or desirable in order to comply with the rules of the United States patent and Trademark Office for recordation of this document.

Assignment
譲渡

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IN WITNESS THEREBY, executed by the undersigned on the date(s) opposite the undersigned Name(s)

年月日	氏名(楷書):	Date	Typed Name
		September 17, 2001	Haruo HYODO
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This assignment may be signed before a U.S. notary Public or before at least two witnesses who also sign here:

年月日	氏名(楷書):	Date	Typed Name
年月日	氏名(楷書):	Date	Typed Name

EXHIBIT V

PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Haruo Hyodo et al.
Appln. No.: 09/963,267 Group Art Unit:
Filed: October 10, 2000 Examiner:
For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir/Madam:

I, Satoshi Watanabe, of Ark Mori Building, 28F, 12-32, Akasaka 1-chome, Minato-ku, Tokyo 107-6028, Japan, hereby state that:

I well understand the Japanese and English languages and attached is an accurate English translation made by me of the Japanese specification in the above-identified U.S. patent application.

Date : July 11, 2003 Name : Satoshi Watanabe

Satoshi WATANABE

EXHIBIT VI

PATENT OFFICE

Japanese Government

This is to certify that the annexed is a true copy of the following application as filed with this office.

Date of Application: October 10, 2003

Application Number: Japanese Patent Application No. 2000-308620

Applicant(s): SANYO ELECTRIC CO., LTD.

Commissioner, Kouzo OKIGAWA
Patent Office:

(Seal)

Issuance No. 2001-3073716

[Document Name] Patent Application

[Reference Number] KAA1000065

[Submission Date] October 10, 2000

[Addressed To] Commissioner, Patent Office

[International Classification] H01L 23/28

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[Indication of Fee]

[Means of Payment] Prepayment

[Registered Number of the Prepayment] 013033

[Amount of Payment] 21000 yen

[List of Attached Documents]

[Article]	Specification	1 copy
[Article]	Drawings	1 copy
[Article]	Abstract	1 copy
[General Power of Attorney Number]		9904451

[Designation of Document] Specification

[Title of the Invention] Semiconductor Device and Method of Manufacturing the Same

[What is claimed is]

[Claim 1] A semiconductor device comprising:

a supporting substrate made of insulating material;

a conductive pattern provided on a surface of the supporting substrate, and external connecting terminals provided on a back surface and connected electrically to the conductive pattern;

a circuit element provided on the conductive pattern;

a glass plate adhered to cover the circuit element and to form an airtight hollow portion between the supporting substrate and the glass plate; and

an adhesive resin applied to an overall adhered surface of the glass plate.

[Claim 2] A semiconductor device according to claim 1, wherein the adhesive resin is formed of a light-shielding adhesive resin.

[Claim 3] A semiconductor device according to claim 1, wherein the circuit element consists of a semiconductor element or a fuse element.

[Claim 4] A semiconductor device manufacturing method comprising:

a step of preparing a supporting substrate in which a

conductive pattern having a large number of mounting portions is provided and external connecting terminals are provided on a back surface;

a step of adhering the circuit element onto the mounting portions respectively;

a step of applying an adhesive resin to an overall adhesive surface of a glass plate that covers the circuit element and forms an airtight hollow portion between the supporting substrate and the glass plate every mounting portion;

a step of adhering the supporting substrate and the glass plate to form the airtight hollow portion every mounting portion; and

a step of separating the supporting substrate every mounting portion by dicing adhered portions between the supporting substrate and the glass plate.

[Claim 5] A semiconductor device manufacturing method according to claim 8, wherein the adhesive resin is formed of a light-shielding adhesive resin.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor device that includes a semiconductor element for high frequency applications and an overcurrent-protecting function in a hollow airtight package and a method of manufacturing the same.

[0002]

[Conventional Art]

An example of the semiconductor device employing the hollow package in the conventional art is shown in FIG.9. This electronic parts comprise a base substrate 1 formed of ceramic, etc., a lead 2 for external connection, and a cap 3 formed similarly of ceramic. A semiconductor chip 5 is adhered onto a surface of an element mounting portion 4 of the lead 2, then the semiconductor chip 5 and the lead 2 are connected via bonding wires 6, and then the semiconductor chip 5 is sealed in an airtight space 7 constructed by the cap 3 (for example, Patent Application Publication Hei 10-173117).

[0003]

Such parts are manufactured via steps of providing the lead 2 in the form of a lead frame, then bonding the semiconductor chip 5 to the lead frame via die bonding or wire bonding, then mounting the base substrate 1 on a bottom surface of the lead frame, then mounting the cap 3 on the base substrate 1 to put the leads 2 between them, and then cutting/shaping the leads 2.

[0004]

[Problems to be Solved by the Invention]

However, in the semiconductor device in the conventional art, there is the subject that, since the base substrate 1 and the cap 3 are mounted on the lead frame every element, the

manufacturing steps become complicated and are not suited for the mass production.

[0005]

Also, there is the problem that, since the semiconductor chip 5 is sealed in the airtight space 7 that is constructed by the cap 3 made of ceramic, etc., the adhesion state cannot be checked by the visual inspection and thus it is difficult to remove the semiconductor device in which the adhesion failure is caused.

[0006]

[Means of Solving the Problems]

A semiconductor device of the present invention has been made in view of the above circumstances, and comprises a supporting substrate made of insulating material, a conductive pattern provided on a surface of the supporting substrate, and external connecting terminals provided on a back surface and connected electrically to the conductive pattern, a circuit element provided on the conductive pattern, a glass plate adhered to cover the circuit element and to form an airtight hollow portion between the supporting substrate and the glass plate, and an adhesive resin applied to an overall adhered surface of the glass plate.

[0007]

Preferably, the semiconductor device of the present invention has such a feature that, since the light-shielding

adhesive resin is applied to the overall adhesive surface of the glass plate that is used to house the circuit element in the airtight hollow space, the state of the adhered portion can be checked by the visual inspection and also the direct incidence of the light onto the circuit element can be prevented, whereby the change in the characteristic of the circuit element can be avoided in structure.

[0008]

In order to overcome the above problems, the semiconductor device manufacturing method of the present invention is characterized by comprising a step of preparing a supporting substrate in which a conductive pattern having a large number of mounting portions is provided and external connecting terminals are provided on a back surface, a step of adhering the circuit element onto the mounting portions respectively, a step of applying an adhesive resin to an overall adhesive surface of a glass plate that covers the circuit element and forms an airtight hollow portion between the supporting substrate and the glass plate every mounting portion, a step of adhering the supporting substrate and the glass plate to form the airtight hollow portion every mounting portion, and a step of separating the supporting substrate every mounting portion by dicing adhered portions between the supporting substrate and the glass plate.

[0009]

Preferably, the semiconductor device manufacturing method of the present invention has such a feature that, since the light-shielding adhesive resin is previously applied to the overall adhesive surface of the glass plate that forms the airtight hollow space in the step of forming the airtight hollow space, a plurality of semiconductor elements can be formed at a time, whereby the manufacturing steps can be simplified and the mass production can be carried out.

[0010]

[Embodiments of the Invention]

Embodiments of the present invention will be explained in detail with reference to the drawings hereinafter.

[0011]

FIG.1 is (A) a sectional view and (B) a plan view showing an embodiment of the semiconductor device of the present invention. A substrate 21a divided from a large-sized substrate 21 is formed of insulating material such as ceramic, glass epoxy, etc., and has a plate thickness of 100 to 300 μm and a rectangular shape whose long side x short side is about 2.5 mm x 1.9 mm when it is viewed as a plan view (viewed as shown in FIG.1(B)). Also, the substrate 21a has a first main face 22a on the surface side and a second main face 22b on the back surface side respectively, and these faces extend in parallel with each other. A portion 23 is an annular pillar portion that is provided on an outer periphery of the substrate 21a to have a height of

about 0.4 mm and a width of about 0.5 mm. A concave portion 24 is formed in the center portion of the substrate 21a by the portion 23. The substrate 21a and the portion 23 both are formed as separate members are adhered by the adhesive 37. In this case, the substrate 21a and the portion 23 both are integrated together previously may be employed.

[0012]

A surface of the first main face 22a of the substrate 21a is formed flat, and an island portion 26 and electrode portions 27, 28 are formed on the surface by conductive patterns such as the gold plating, or the like. Then, a semiconductor chip 29 such as a Schottky barrier diode, a MOSFET element, or the like, for example, is die-bonded to the island portion 26 of the substrate 21a. An electrode pad formed on a surface of the semiconductor chip 29 and the electrode portions 27, 28 are connected by bonding wires 30.

[0013]

External connecting terminals 32, 33, 34 are formed on the surface of the second main face 22b of the substrate 21a by the conductive patterns such as the gold plating, or the like. In addition, a via hole 35 that passes through the substrate 21a from the first main face 22a to the second main face 22b is provided in the electrode portions 32, 33, 34. An inside of the via hole 35 is filled with conductive material such as tungsten, silver, copper, or the like, so that the island

portion 26, the electrode portion 27, and the electrode portion 28 are connected electrically to the external connecting terminal 32, the external connecting terminal 33, and the external connecting terminal 34 respectively. End portions of the external connecting terminals 32, 33, 34 are retreated from the end portion of the substrate 21a by about 0.01 to 0.1 mm. Also, since upper surfaces of the via holes 35 of the electrode portion 27, 28 are not flat, it is preferable that the bonding wire 30 should be connected to avoid the upper surfaces of the via holes 35 of the electrode portion 27, 28 respectively. The external connecting terminals 32, 33, 34 are formed in advance on the large-sized substrate 21.

[0014]

In order to form the inside of the concave portion 24 as a closed space, a transparent glass plate 36 having a plate thickness of about 0.1 to 0.3 mm is employed as a lid member. Since the glass plate 36 covers a number of concave portions 24 formed on the large-sized substrate 21, the light-shielding adhesive resin 37 is previously applied to the overall adhered surface of the glass plate 36. Also, since the upper portion of the column portion 23 forming the concave portion 24 and the adhered surface of the glass plate 36 are adhered, the semiconductor chip 29 and the metal thin wire 30 can be housed perfectly in the airtight space.

[0015]

Here, since the light-shielding adhesive resin 37 is applied to the overall adhered surface of the glass plate 36, the light that transmits the glass plate 36 can be cut off by the light-shielding adhesive resin 37 and thus the light does not directly enter into the semiconductor chip 29, etc. in the concave portion 24.

[0016]

The column portion 23 cut by the dicing surrounds the peripheral area of the semiconductor chip 29, and the cut glass plate 36 closes tightly the upper area thereof. The column portion 23 and the first main face 22a of the substrate 21a are adhered by the adhesive 37, and the column portion 23 and the glass plate 36 are adhered by the adhesive 37. As a result, the semiconductor chip 29 and the metal thin wires 30 are housed in the airtight space constructed by the concave portion 24. Outer peripheral end surfaces of the substrate 21a, the column portion 23, and the glass plate 36 are cut by the dicing so as to form flat cut end surfaces.

[0017]

The above semiconductor device is mounted such that the external connecting terminals 32, 33, 34 are opposed/adhered to the electrode patterns on the packaging substrate.

[0018]

Here, an embodiment in which respective semiconductor chips that are adhered onto respective mounting portions are

covered with a common resin layer by covering a resin layer with the substrate will be explained in brief.

[0019]

The large-sized substrate in which a plurality of mounting portions are arranged in a matrix fashion, e.g., 100 portions are arranged in 10 rows and 10 columns, on the substrate having the plate thickness of 200 to 350 μm that can maintain the mechanical strength during the manufacturing steps is prepared. The substrate is an insulating substrate made of ceramic, glass epoxy, or the like. Then, the semiconductor chips are die-bonded to respective mounting portions and then all semiconductor chips are covered with the common resin layer by dropping (potting) epoxy liquid resin by a predetermined amount. After the dropped resin layer is cured by the heat treatment executed at 100 to 200 degree for several hours, a surface of the resin layer is worked into a flat surface by grinding curved surfaces. In the grinding, the dicing apparatus is used to grind the surface of the resin layer by the dicing blade such that the surface of the resin layer has a uniform height from the substrate. In this step, a film thickness of the resin layer is formed to 0.3 to 1.0 mm. The blades having various plate thicknesses are prepared, and the overall surface of the resin layer is formed into a flat surface by repeating cutting several times while using the relatively thick blade.

[0020]

Next, FIG.2 is (A) a sectional view and (B) a plan view showing an embodiment of an overcurrent-protecting device using a fuse. A substrate 51 is formed of insulating material such as ceramic, glass epoxy, etc. The substrate 51 has a plate thickness of 100 to 300 μm and a rectangular shape whose long side x short side is about 2.5 mm x 1.9 mm when it is viewed as a plan view (viewed as shown in FIG.2(B)). Also, the substrate 51 has a first main face 52a on the surface side and a second main face 52b on the back surface side respectively. A column portion 53 is an side portion that is provided on an outer periphery of the substrate 51 to have a height of about 0.4 mm and a width of about 0.5 mm. A concave portion 54 is formed on the center portion of the substrate 51 by the column portion 53. The substrate 51 and the column portion 53 both are formed as separate members are adhered by the adhesive 61. In this case, the substrate 51 and the column portion 53 both are integrated together previously may be employed.

[0021]

A surface of the first main face 52a of the substrate 51 is formed flat, and electrode portions 55, 56 are formed on the surface by conductive patterns such as the gold plating, or the like. A metal thin wire 57 having a diameter of 30 μm, for example, is provided between the electrode portions 55, 56 by the wire bonding. The metal thin wire 57 is formed of a gold wire having a purity of 99.99 %, a solder thin wire,

or the like. The metal thin wire 57 is first bonded to the electrode portion 55 and is second bonded to the electrode portion 56 such that a wire loop is formed to have a height smaller than a height of the concave portion 54.

[0022]

External connecting terminals 58, 59 are formed on the surface of the second main face 52b of the substrate 51 by the conductive patterns such as the gold plating, or the like. In addition, a via hole 60 passing through the substrate 51 is provided under the electrode portions 55, 56 respectively. An inside of the via hole 60 is filled with conductive material such as tungsten, or the like, so that the electrode portion 55 and the electrode portion 56 are connected electrically to the external connecting terminal 58 and the external connecting terminal 59 respectively. End portions of the external connecting terminals 58, 59 are retreated from the end portion of the substrate 51 by about 0.01 to 0.1 mm. Also, since upper surfaces of the via holes 60 of the electrode portion 55, 56 are not flat, it is preferable that the bonding wire 57 should be connected to avoid the upper surfaces of the via holes 60 of the electrode portion 55, 56 respectively.

[0023]

In order to form the inside of the concave portion 54 as a closed space, a transparent glass plate 62 having a plate thickness of about 0.1 to 0.3 mm is employed as a lid member.

Since the glass plate 62 covers a number of concave portions 54 formed on the large-sized substrate 21, the light-shielding adhesive resin 61 is previously applied to the overall adhered surface of the glass plate 62. Also, since the upper portion of the column portion 53 forming the concave portion 54 and the adhered surface of the glass plate 62 are adhered, the metal thin wire 57 can be housed perfectly in the airtight space.

[0024]

Here, since the light-shielding adhesive resin 61 is applied to the overall adhered surface of the glass plate 62, the light that transmits the glass plate 62 can be cut off by the light-shielding adhesive resin 61 and thus the light does not directly enter into the metal thin wire 57, etc. in the concave portion 54.

[0025]

The above overcurrent-protecting device is mounted such that the external connecting terminals 58, 59 are opposed/adhered to the electrode patterns on the packaging substrate. When an overcurrent in excess of the rated current is flown between the external connecting terminals 58, 59, such overcurrent flows through the metal thin wire 57 to cause the rapid temperature rise due to the specific resistance of the metal thin wire 57. The metal thin wire 57 is melt down by this heat generation to perform a protection function against the overcurrent. If a gold (Au) wire having the diameter of

30 μm and a wire length of about 0.7 mm is employed, the fusing current is about 4 A (1 to 5 seconds). In many cases, because of the relationship between the radiation and the resistance, the metal thin wire 57 is melt down in its middle portion rather than its end portions close to the electrode portions 55, 56. At this time, since the fused portion does not contact to other material such as the resin, the device in which the ignition, the emitting smoke, the change of color, and the deformation are not generated in appearance can be obtained. Also, since the metal thin wire 57 is melted down, the device in which both terminals are disconnected perfectly at the time of the overcurrent can be formed.

[0026]

The fuse element can be formed by forming a part of the conductive patterns constituting the electrode portions 55, 56 as a narrow wedge-like shape successively, by adhering a polysilicon resistor to the metal thin wire, or the like in addition to the metal thin wire. In summary, any means may be employed if the fused portion is housed in the concave portion 54. Also, although the concave portion 54 is airtightly closed in the air, the incombustible gas to form the nitrogen atmosphere, etc., for example, can be filled therein.

[0027]

As described above, according to the semiconductor device of the present invention, since the transparent glass plate

36 is employed to seal the semiconductor chip 29, the bonding wires 30, etc. airtightly in the hollow space, the state of the adhered portion between the glass plate 36 and the column portion 23 can be checked by the visual inspection. Also, since the light-shielding adhesive resin 37 is applied to the entire adhered surface of the glass plate 36, there can be prevented such an event that the light that transmits through the glass plate 36, enters into the concave portion 24 and directly enters into the semiconductor chip 29, etc. and thus the degradation of the characteristic of the semiconductor chip 29, etc. is caused.

[0028]

In addition, in the semiconductor device of the present invention, the hollow structure can be formed by employing the column portion 23 and the glass plate 36, and also the semiconductor chip 29, etc. that are die-bonded onto the substrate 21a are housed in the airtight space constructed by the concave portion 24 as the hollow portion. Accordingly, a material cost can be lowered extremely in contrast to the case where the substrate 21a is covered with the resin layer and therefore the semiconductor chips 29 adhered onto the mounting portions are covered with the resin layer.

[0029]

Further, in the semiconductor device of the present invention, the hollow structure can be formed by using the column

portion 23 and the glass plate 36 and also the step of planarizing the surface of the semiconductor element is not needed because the glass plate 36 is employed as the lid body of the hollow structure. Therefore, a production cost can be lowered extremely rather than the case where the substrate 21a is covered with the resin layer and therefore the semiconductor chips 29 adhered onto the mounting portions are covered with the resin layer.

[0030]

Besides, the via holes 35 passing through the substrate 21a from the first main face 22a to the second main face 22b are formed in the substrate 21a. Then, the insides of the via holes 35 are filled with the conductive material such as tungsten, silver, copper, etc., and also the island portion 26, the electrode portion 27, and the electrode portion 28 are connected electrically to the external connecting terminals 32, 33, 34 respectively, so that internal elements and the external connecting terminals can be connected electrically with no lead that is extended from the substrate 21a to the outside. Therefore, a packaging area can be reduced extremely when the semiconductor device is packaged onto the printed board.

[0031]

A first embodiment of the present invention shown in FIG.1 will be explained in detail hereinafter.

[0032]

First step: see FIG.3(A)

At first, the large-sized substrate 21 is prepared. The large-sized substrate 21 is formed of insulating material such as ceramic, glass epoxy, etc. and has a plate thickness of 100 to 300 μm. Also, the large-sized substrate 21 has the first main face 22a on the surface side and the second main face 22b on the back surface side respectively. A symbol 23 is a lattice-like column portion having a height of 0.1 to 0.5 mm and a constant width of about 0.25 to 0.5 mm, and forms the concave portion 24 in which the center portion of the substrate 21 is depressed by the column portion 23. The substrate 21 and the column portion 23 are formed integrally in advance to form the above plate thickness including the column portion 23. In this case, the structure in which the substrate 21 and the column portion 23 are formed individually and then adhered/fixed together may be prepared.

[0033]

The concave portions 24 each having a size of about 0.8 mm x 0.6 mm, for example, are arranged at an equal distance vertically and laterally on the substrate 21. A large number of sets of the island portions 26 and the electrode portions 27, 28 are drawn on the first main faces 22a of the concave portions 24 by the conductive patterns formed of the gold plating. The concave portion 24 and a part of the column portion 23 of the second substrate 21b surrounding the concave portion 24

constitute the element mounting portion 41.

[0034]

Second step: see FIG.3(B)

After such substrate 21 is prepared, the semiconductor chip 29 is die-bonded to the island portion 26 every concave portion 24 and the bonding wire 30 is wire-bonded. Then, one sides of the bonding wires 30 that are wire-bonded to the semiconductor chip 29 are connected to the electrode portions 27, 28. A loop height of the bonding wire 30 at this time is set to a height that is lower than a height of the column portion 23.

[0035]

Third step: see FIG.4(A)(B)

The transparent glass plate 36 having a plate thickness of about 0.1 to 0.3 mm is prepared, and then the light- shielding adhesive resin 37 is applied to the overall adhered surface of the glass plate 36. Then, the glass plate 36 is adhered as a lid member that constitutes the hollow airtight structures on the mounting portions 41 including a plurality of concave portions 24 that are formed by using the large-sized substrate 21 and the column portions 23. Accordingly, the semiconductor chip 29 and the bonding wire 30 can be perfectly housed in the airtight space. At this time, as described above, since the light-shielding adhesive resin 37 is applied to the overall surface of the glass plate 36, a large quantity of semiconductor

elements can be formed at a time.

[0036]

Here, the column portion 23 may be adhered to the large-sized substrate 21 later, otherwise the large-sized substrate 21 and the column portion 23 may be integrally formed together previously. Also, the concave portions 24 may be formed by digging the large-sized substrate 21.

[0037]

After this, it is visually checked whether or not the adhesion failure is caused between the column portion 23 and the glass plate 36.

[0038]

Fourth step: see FIG.4(C)

Then, individual devices shown in FIG.5 can be obtained by dividing the substrate 21 into respective mounting portions 41 based on alignment marks formed on the surface of the substrate 21. A dicing blade 42 is used to divide, and a dicing sheet is pasted on the back surface side of the substrate 21 and then the substrate 21 and the glass plate 36 are collectively cut away along dicing lines 43 vertically and laterally. In this case, the dicing line 43 is positioned in the center of the column portion 23. Also, the dicing sheet may be pasted on the glass plate 36 side and then the dicing may be applied from the second main face 22b side.

[0039]

A second embodiment of the present invention shown in FIG.1 will be explained in detail hereinafter. This is the case where the column portion 23 is constructed as the discrete parts.

[0040]

First step: see FIG.6(A)

At first, the large-sized flat substrate 21 is prepared. The large-sized substrate 21 is formed of insulating material such as ceramic, glass epoxy, etc. and has a plate thickness of 100 to 300 μm. Also, the large-sized substrate 21 has the first main face 22a on the surface side and the second main face 22b on the back surface side respectively. A large number of sets of the island portions 26 and the electrode portions 27, 28 are drawn on the surface of the first main faces 22a by the conductive patterns formed of the gold plating. The area that surrounds the island portion 26 and the electrode portions 27, 28 constitutes the element mounting portion 41. A large number of element mounting portions 41 are arranged at an equal distance vertically and laterally.

[0041]

Second step: see FIG.6(B)

After such substrate 21 is prepared, the semiconductor chip 29 is die-bonded to the island portion 26 every element mounting portion 41 and the bonding wire 30 is wire-bonded. Then, one sides of the bonding wires 30 that are wire-bonded

to the semiconductor chip 29 are connected to the electrode portions 27, 28. A loop height of the bonding wire 30 at this time is set to a height that is smaller than a depth of the concave portion 24.

[0042]

Third step: see FIG.7(A)

The second substrate 21a having the concave portions 24 (through holes) at positions that correspond to the element mounting portions 41 is adhered/fixed to the surface of the first main face 22a on the substrate 21 to which the die bonding and the wire bonding have been applied. The adhesive such as epoxy adhesive, etc. is employed to adhere.

[0043]

The concave portions 24 each having a size of about 0.8 mm x 0.6 mm, for example, are arranged at an equal distance vertically and laterally on the second substrate 21b. The column portion 23 having a height of about 0.1 to 0.2 mm and a width of about 0.2 to 0.5 mm is provided between the concave portions 24 so as to surround the concave portion 24 in a lattice fashion. As a result, the island 26, the semiconductor chip 29, the electrode portions 27, 28, etc. are exposed from the concave portion 24, which is equivalent to the state in FIG.3(B). According to this approach, since the die bonding and the wire bonding can be applied to the flat substrate 21, the contact between the vacuum collet or the bonding tool and the column

portion 23 can be eliminated and thus a dimension of the concave portion 24 can be reduced.

[0044]

Fourth step: see FIG.7(B)(C)

The transparent glass plate 36 having a plate thickness of about 0.1 to 0.3 mm is prepared, and then the light- shielding adhesive resin 37 is applied to the overall adhered surface of the glass plate 36. Then, the glass plate 36 is adhered as a lid member that constitutes the hollow airtight structures on the mounting portions 41 including a plurality of concave portions 24 that are formed by using the large-sized substrate 21 and the column portions 23. As a result, the semiconductor chip 29 and the bonding wire 30 can be perfectly housed in the airtight space. At this time, as described above, since the light-shielding adhesive resin 37 is applied to the overall surface of the glass plate 36, a large quantity of semiconductor elements can be formed at a time.

[0045]

After this, it is visually checked whether or not the adhesion failure is caused between the column portion 23 and the glass plate 36.

[0046]

Fifth step: see FIG.8(A)

Then, individual devices shown in FIG.8(B) can be obtained by dividing the substrate 21 into respective mounting

portions 41 based on alignment marks formed on the surface of the substrate 21. The dicing blade 42 is used to divide, and the dicing sheet is pasted on the second main face 22b side of the substrate 21 and then the substrate 21, the second substrate 21b, and the glass plate 36 are collectively cut away along the dicing lines 43 vertically and laterally. In this case, the dicing line 43 is positioned in the center of the column portion 23. Also, the dicing may be applied from the second main face 22b side.

[0047]

[Advantages of the Invention]

As described above, according to the semiconductor device of the present invention, since the transparent glass plate is employed to seal the semiconductor chip, the bonding wires, etc. airtightly in the hollow space, the state of the adhered portion between the glass plate and the column portion can be checked by the visual inspection. Also, since the light-shielding adhesive resin is applied to the entire surface of the adhered surface of the glass plate, there can be prevented such an event that the light that transmits through the glass plate, enters into the concave portion and directly enters into the semiconductor chip, etc. and thus the degradation of the characteristic of the semiconductor chip, etc. is caused.

[0048]

In addition, according to the semiconductor device

manufacturing method of the present invention, since the light-shielding adhesive resin is previously applied to the overall adhesive surface of the glass plate that forms the hollow airtight structure, the semiconductor element, etc. can be adhered at a time onto a number of concave portions that are constructed by the substrate and the column portions. Therefore, the fabrication cost can be reduced extremely and the mass production can be carried out.

[Brief Description of the Drawings]

[FIG.1]

(A) is a sectional view and (B) is a plan view showing the present invention.

[FIG.2]

(A) is a sectional view and (B) is a plan view showing the present invention.

[FIG.3]

(A) is a perspective view and (B) is a perspective view showing the present invention.

[FIG.4]

(A) is a sectional view, (B) is a perspective view, and (C) is a perspective view showing the present invention.

[FIG.5]

A perspective view showing the present invention.

[FIG.6]

(A) is a perspective view and (B) is a perspective view showing the present invention.

[FIG.7]

(A) is a perspective view, (B) is a sectional view, and (C) is a perspective view showing the present invention.

[FIG.8]

(A) is a perspective view and (B) is a perspective view showing the present invention.

[FIG.9]

(A) is a sectional view and (B) is a plan view showing an example in the conventional art

[Designation of Document] Abstract

[Abstract]

[Problem] In a semiconductor device in which semiconductor devices for high-frequency applications are housed in a hollow airtight package, the present invention relates to a semiconductor device employing a glass plate as a lid body of the hollow airtight package, and a method of manufacturing the same.

[Solving Means] The present invention comprises a first main face 22a on the surface side of a substrate 21a. An island portion 26 is formed on the first main face 22a and a semiconductor chip 29, etc. are adhered onto the first main face 22a. The semiconductor chip 29, etc. are sealed in a hollow space made by a column portion 23 and a transparent glass plate 36. Then, the column portion 23 and the glass plate 36 are adhered by the light-shielding adhesive resin made of epoxy resin. Accordingly, there can be provided the semiconductor device and a method of manufacturing the same, which can prevent the direct incidence of the light onto the semiconductor chip 29 and the degradation of the characteristic of the semiconductor chip 29 can be suppressed.

[Selected Drawing] FIG.1

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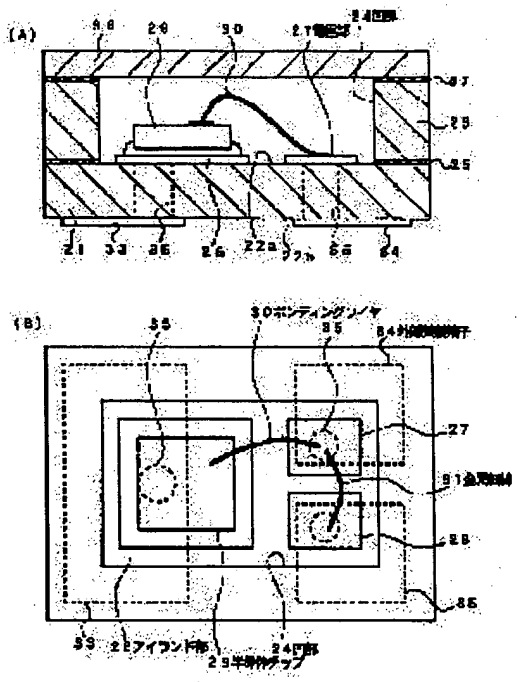
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE OF THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a semiconductor device possessed of a built-in fuse element which is kept free of ignition, fuming, and deformation.
SOLUTION: An island 26 and electrodes 27 and 28 are formed on the surface of a board 21, and a semiconductor chip 29 is fixed to the island 26. A wire is bonded between an electrode pad and the electrode 27, and furthermore a metal fine wire 31 is connected between the electrodes 27 and 28 to serve as a fuse element. Via holes 35 are bored in the board 21 to lead the islands 26 and the electrodes 27 and 28 out each to outer connection terminals 33, 34, and 35. A columnar part 23 is provided on the periphery of the board 24, by which a recess 24 surrounded with the columnar part 23 is formed, and a metal fine wire 31 is housed in the recess 24. The recess 24 is hermetically sealed with a lid 36 put on its upper opening. The fuse element is housed in the recess 24, and the fuse is restrained from coming into contact with resin or the like, so that the fuse element will not ignite, fume, or deform.



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